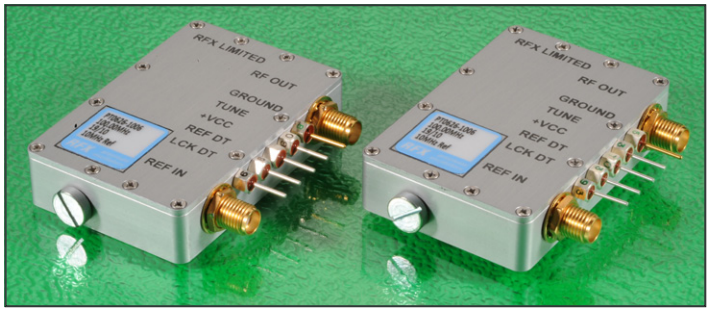
1MHz to 2.4GHz PLL hybrid OCXO module phase locked to external 10.00MHz precision reference

sine wave output, 0dBm into 50Ω

Hermetically sealed case, 13mm height

h.f. Communications equipment, system synchronisation, precision reference



Generic specification:

Stability:

OCXO holdover	*from ±0.005ppm(0 +50)°C, custom specified*
locked	*dependent upon input reference accuracy*
input reference	*10.000MHz, 0dBm, as standard, +2dBm ±6dB*
against V_{cc} change	*±0.002ppm max., V_{cc} ±5%*
against load change	*±0.0002ppm max., load ±10%*
ageing short term	*±0.0003ppm max./day after 30 days continuous operation*
ageing long term	*from ±0.1ppm max./ year after 30 days continuous operation*
electronic trim	*±1.0ppm min, no reference*
Output:	*sine wave, +0dBm min. harmonics -25dBc*

Power supplies:

supply voltage	*+5Vd.c. ±5%*
start up current	*560mA max.*
quiescent current	*270mA max. at +25°C*
warm up time	*4 minutes max. to within ±0.1ppm of nominal*

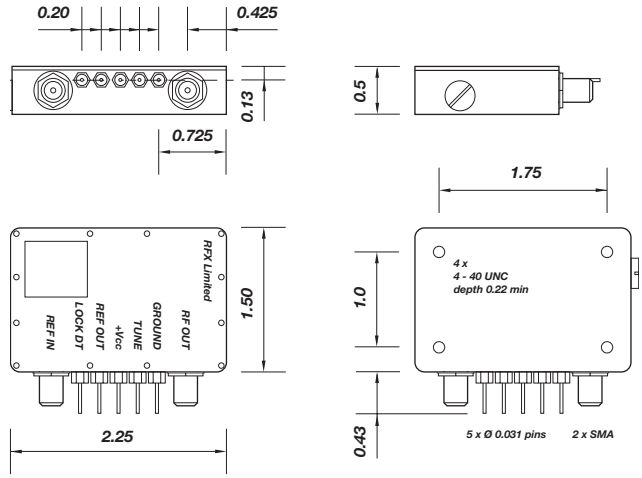
Typical free run phase noise:

single sideband, 1Hz bandwidth	*-105dBc/Hz, f_o +10Hz* *-120dBc/Hz, f_o +100Hz* *-135dBc/Hz, f_o +1kHz* *-155dBc/Hz, f_o +10kHz* *phase noise at lock dependent on reference input*
Jitter:	*<1ps*

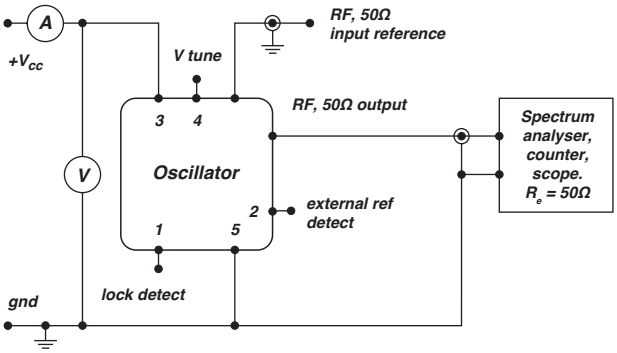
Temperature:

operating range	*(0 +50)°C*
storage range	*(-40 +125)°C*
Insulation resistance:	*500MΩ min., 100Vd.c.*
Marking:	*part number, frequency, date code, serial number*

Dimensions(inches):



Test circuit:



Lock detect levels:
CMOS: low; no lock, high; lock

External ref detect levels:
CMOS: low; no reference, high; ref detected

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