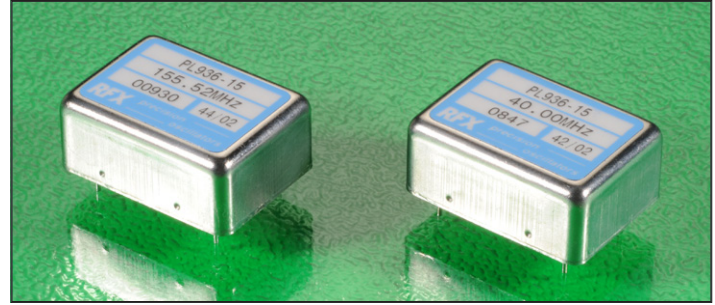


1MHz to 2.4GHz phase locked loop hybrid TCXO module phase locked to external precision reference.

ECL, sine wave output, sub 1ps jitter.

Hermetically sealed case, 15mm height.

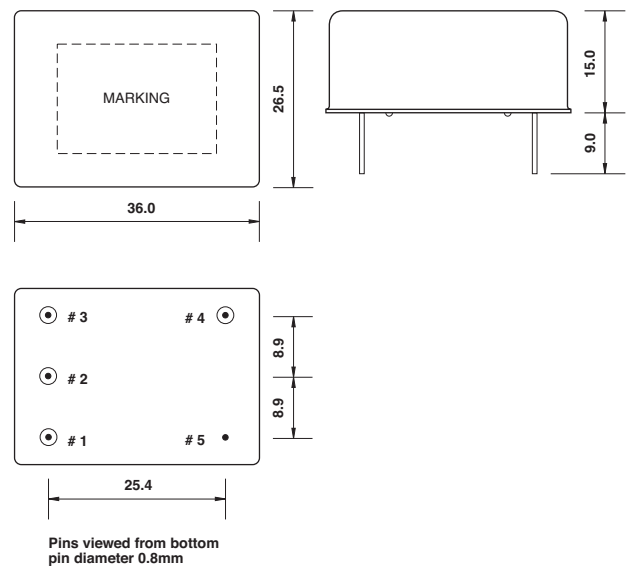
h.f communications equipment, system synchronisation.



**Generic specification:**

<b>frequency range:</b>	1MHz ~ 2.4GHz
<b>stability:</b>	
TCXO holdover	from $\pm 1$ ppm, custom specified
locked	dependent upon input reference accuracy
input reference	10.000MHz, 0dBm, as standard
against $V_{cc}$ change	$\pm 0.05$ ppm max., $V_{cc} \pm 5\%$
against load change	$\pm 0.02$ ppm max., load $\pm 10\%$
ageing short term	$\pm 0.005$ ppm max./day
ageing long term	from $\pm 5$ ppm max. 10 years
<b>output:</b>	single ended PECL, sine wave, CMOS
lock time	30secs max., frequency dependent
<b>supply voltage:</b>	+3.3Vd.c., +5Vd.c., +12Vd.c., $\pm 5\%$
<b>supply current:</b>	50mA typical, frequency dependent
<b>insulation resistance:</b>	500M $\Omega$ min., 100Vd.c.
<b>typical phase noise:</b>	
single sideband, 1Hz bandwidth	-100dBc/Hz, $f_o + 10$ Hz -115dBc/Hz, $f_o + 100$ Hz -125dBc/Hz, $f_o + 1$ kHz
<b>jitter:</b>	1ps max., typical
<b>temperature:</b>	
operating range	customer specified
storage range	(-40 +125) $^{\circ}$ C
<b>marking:</b>	part number, frequency, date code, serial number

**Dimensions(mm):**



**Pin connections:**

- #1 RF input reference frequency
- #2 lock detect output
- #3 supply voltage,  $V_{cc}$
- #4 RF output
- #5 ground/case

**Test circuit:**

